IN THE SPECIFICATION

At page 1, in the paragraph previously inserted between prenumbered lines 2 and 4 in the previously filed Preliminary Amendment, please amend that paragraph as follows:

CROSS-REFERENCE TO RELATED APPLICATION

The present patent document is a divisional of co-pending U.S. application serial no. 10/093,933, filed on March 11, 2002, now U.S. patent 6,727,724, which in turn is a continuation of U.S. application serial no. 09/714,148 filed on November 17, 2000, now U.S. patent 6,373,274, which in turn is a continuation of U.S. application serial no. 09/249,139 filed on February 12, 1999, now U.S. patent 6,169,415, the entire contents of each of which are hereby incorporated herein by reference.

Please replace the paragraph at page 12, lines 18-21, with the following rewritten paragraph:

The characteristic evaluation apparatus of the eleventh aspect facilitates ~~to determine~~ determining the value of channel narrowing when the first and second gate overdrives are in the vicinity of zero because the stationary point of the second estimated value is present in the vicinity of zero.

Please replace the paragraph at page 13, lines 4-7, with the following rewritten paragraph:

The characteristic evaluation apparatus of the seventh, eighth or seventeenth aspect facilitates ~~to determine~~ determining true threshold voltages because the second characteristic curves that are obtained for the true threshold voltage on a graph may approximately coincide, irrespective of mask channel width.

Please replace the paragraph beginning at page 33, line 13 to page 34, line 1, with the following rewritten paragraph:

In the channel narrowing DW extraction according to the first or second preferred embodiment, when the mask ~~cannel~~ channel width W_{mNa} of a narrow transistor is significantly smaller than the mask ~~cannel~~ channel width W_{mWi} of a wide transistor (i.e., $W_{mNa}<<W_{mWi}$), the difference between the mask channel width W_{mwi} and a gate finished width W_{gWi} hardly affects [[on]] determination of the value DW^* of W_m coordinate at a virtual point, and thereby determines the channel narrowing DW of the narrow transistor at high accuracy. For instance, to evaluate device or circuit performance on the level of not more than 1.0 μm in pattern width, it is required to extract the channel narrowing DW of each transistor. For such an extraction, there are used two transistors, i.e., a narrow transistor and a wide transistor serving as a reference. In this case, the difference between a gate finished width W_g and a mask channel width W_m depends on the transistor, causing an error. Thus, description will be now given of such an error. The value dW^{**} of W_m coordinate at a virtual point when a mask channel width W_m is used is given by Equation 20.

Please replace the paragraph at page 52, lines 8-16, with the following rewritten paragraph:

Also, the presence of the stationary point at V_{gt}=O suggests the possibility that δ W is determined so that $DW^{\#}$ is constant when V_{gt} is in the vicinity of zero. This is the case ~~where~~ in which a "shift and ratio method" is applied to the extraction of a channel narrowing DW (this method is described, for example, in "A New "Shift and Ratio" Method for MOSFT Channel Length Extraction," IEEE Elect. Dev. Lett., EDL-13(5), p.267, 1992, by Y. Taur et al.). This method actually gives proper values, however, its extraction result depends greatly on the area of a gate overdrive V_{gt} for calculation (see Fig. 29). On the other hand, both the

Rm method and the Gm method are independent of the area of a gate overdrive V_{gt} for calculation, and also can give nearly the same result.